Electrode modulated capacitance-electric field nonlinearity in metal-insulator-metal capacitors

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Metals with low enthalpy of oxide formation (ΔH_{ox}) are used to examine the influence of the metal/dielectric interface, in the absence of a significant interfacial layer oxide (ILO), on the voltage nonlinearity of capacitance for metal-insulator-metal capacitors. For both atomic layer deposited Al_2O_3 and HfO_2 dielectrics, Ag electrode devices show the lowest quadratic electric field coefficient of capacitance (α_{ECC}), followed in increasing order by Au, Pd, and Ni. The difference between the metals is greater for thinner dielectrics, which is consistent with increased influence of the interface. In addition, with decreasing dielectric thickness the quadratic voltage field coefficient of capacitance increases, whereas α_{ECC} decreases. It is proposed that the thickness dependencies are due to an interaction between vertical compression of the dielectric under an applied bias and the concomitant lateral expansion induced stress that is concentrated near the interface. Through this interaction, the metal interface inhibits lateral expansion of the dielectric resulting in a reduced α_{ECC}. Indeed, α_{ECC} is found to increase with the increasing lattice mismatch at the metal/dielectric interface, likely due to edge dislocations. Finally, Al, a high ΔH_{ox} metal, is found to fit the trend for Al_2O_3 but not for HfO_2, due to the formation of a thin reduced-k ILO at the HfO_2/Al interface. These results suggest that minimization of metal/dielectric lattice mismatch may be a route to ultra-low nonlinearity in highly scaled metal-insulator-metal devices. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4989531]

Future nodes of back-end-of-line (BEOL) metal-insulator-metal capacitors (MIMCAPs) for use in analog and mixed signal (AMS) applications require ever-increasing capacitance density (C) while maintaining low leakage current density (J) and low nonlinearity (characterized by the quadratic voltage coefficient of capacitance, α_{VCC}), as projected by the International Technology Roadmap for Semiconductors (ITRS).[1] Scaling down the size of these MIMCAPs has proven challenging as C, J, and α_{VCC} are all inversely related to the dielectric thickness (d_{ox}).[2–4] AMS applications are particularly sensitive to α_{VCC}, which is determined empirically by fitting a parabolic expression to the capacitance vs. the voltage measurement

$$\Delta C/C_0 = \alpha_{VCC} V^2 + \beta_{VCC} V, \quad (1)$$

where C_0 is the capacitance density at 0 V, $\Delta C = C(V) - C_0$ is the change in capacitance at a given applied bias, and β_{VCC} is the linear voltage coefficient of capacitance. C_0 is characterized by the parallel plate capacitor equation, $C_0 = \frac{\varepsilon_0 \kappa}{d_{ox}}$, where ε_0 is the permittivity of vacuum and κ is the dielectric constant. It is well established that the "bulk" dielectric material has a dominant effect on α_{VCC}, which increases with the increasing dielectric constant and roughly with $1/d_{ox}^2$.[4–6] However, despite its technological importance, the fundamental mechanisms responsible for α_{VCC} are not fully understood. The mechanisms that have been proposed include non-linear metal-oxygen bond polarizability,[5,6] dielectric thermal expansion,[7] free carrier injection into oxygen vacancies creating a double layer,[8–12] and induced film strain from electrostriction and Maxwell stress.[3,13,14] Of the few studies that have considered the impact of the electrodes on α_{VCC}, most have focused on interfacial layer oxides (ILOs).[3,8,9,12,13] Although they may play a substantial role when present, ILOs alone cannot fully explain the variation between electrodes. For example, metals that are unlikely to form significant oxides, those that have low enthalpy of oxide formation (ΔH_{ox}), still exhibit differing α_{VCC} values for the same dielectric.[9] Thus, in addition to ILOs, the metal electrodes themselves must exert an influence on α_{VCC}. An increased understanding of the role of the electrode interfaces in influencing α_{VCC} is needed to enable development and optimization of low α_{VCC} MIMCAPs for future technology generations.

In this work, metals with low ΔH_{ox} are used to examine the influence of the top electrode interface, in the absence of a significant ILO, on the nonlinearity of MIMCAPs with the same bottom electrode and atomic layer deposited (ALD) dielectrics of various thickness. Comparison is made with relatively high ΔH_{ox} Al electrode devices to look at the impact of ILOs on voltage nonlinearity. Finally, the observed dependence of α_{ECC} on the electrode material and dielectric thickness is qualitatively explained with interfacial stress and metal-dielectric lattice mismatch.

For the metal-insulator-metal (MIM) devices used in this work, substrates of Si/SiO_2 (550 nm)/Ta (20 nm)/TaN (150 nm) with the TaN layer planarized via chemical mechanical polishing were provided by ON Semiconductor and used as the bottom electrodes. ALD of amorphous Al_2O_3 and HfO_2 thin films was performed in Picosun SUNALE R-200 and R-150 reactors, respectively, at a chamber

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temperature of 250 °C using alternating N_2-purge-separated pulses of H_2O and either trimethylaluminum (TMA) or tetrakis[ethylmethylamino]hafnium (TEMA-Hf). The TMA source was maintained at ~17 °C, and TEMA-Hf was held at 90 °C. The growth per cycle (GPC) of Al_2O_3 and HfO_2 was 0.92 nm/cycle and 0.77 nm/cycle, respectively. Au, Ag, Pd, Ni, and Al top metal electrodes were deposited via thermal evaporation. The film thickness was measured using a J.A. Woollam M2000 spectroscopic ellipsometer (SE) in the range of 400–1000 nm. Electrical measurements were taken using a B1500A semiconductor device parameter analyzer and an E4980A LCR meter. All electrical tests were conducted with the bottom electrode held at ground and performed in the dark at room temperature.

Shown in Fig. 1(a) is a plot of normalized capacitance (C/C_0) vs. voltage for TaN/Al_2O_3/Ag MIMCAPs with 10, 21, and 41.5 nm of Al_2O_3. In this figure, the linear baseline [β_{VCC} term from Eq. (1)] has been removed. ALD Al_2O_3 shows a positive α_{VCC} (C increases with V) value that increases in magnitude as dielectric thickness decreases, which is a trend commonly displayed by dielectric materials.[15–17] Assuming that nonlinearity is purely a "bulk" dielectric effect, then normalizing for d_{ox}, the extracted *electric field* coefficient of capacitance (α_{ECC}) should be independent of d_{ox} (α_{ECC} should remain constant for all Al_2O_3 thicknesses). However, when the same data are plotted vs. electric field (E), as shown in Fig. 1(b), we find that α_{ECC} decreases with the decreasing d_{ox} value. This behavior is not predicted by existing models and indicates either (i) the presence of an ILO or (ii) the influence of a non-bulk interfacial mechanism.[3,5,7,10]

A dielectric thickness dependence of α_{ECC} can be generated by an ILO. To determine whether an ILO is present, the zero-bias capacitance equivalent oxide thickness (CET, defined as $\varepsilon_{SiO2}/C_{TOT}$) is plotted vs. the measured optical thickness in Fig. 1(c). If the thickness of the hypothetical ILO stays relatively constant with respect to the thickness of the deposited dielectric, then the ILO acts as a constant series capacitance, with the total capacitance, C_{TOT}, calculated via

$$C_{TOT} = \frac{C_d * C_{ILO}}{C_d + C_{ILO}}, \tag{2}$$

where C_d is the capacitance of the deposited dielectric and C_{ILO} is the capacitance of the ILO. The slope of this plot is then proportional to the κ of the deposited dielectric, and the y-intercept of a linear extrapolation indicates the CET of the ILO. The slope of a linear fit indicates $\kappa_{Al2O3} = 7.88$ and extrapolates approximately back to the origin, suggesting the absence of a *capacitive* ILO (any ILO that is present must be conductive and not contribute to capacitance).[18] Identical results were obtained using other voltages. Note that TaN was chosen as a lower electrode as it is commonly used in industry for MIM capacitors. Within the temperature limits of BEOL processing, TaN is an effective diffusion barrier to copper, exhibits small metal diffusion into dielectrics, and displays relatively small changes in resistance when oxidized.[19–21] Therefore, any ILO that develops at the TaN interface is likely conductive. For the top electrode, ~320 nm of Ag was used. Ag has a very small ΔH_{ox} and should not introduce an ILO at the top interface.[22] Thus, the α_{ECC} dependence on d_{ox} observed in Fig. 1(b) is unlikely to be the result of an ILO at either electrode but rather due to another interaction at the metal-dielectric interface.

Shown in Fig. 2 are plots of α_{ECC} versus dielectric film thickness for ALD (a) Al_2O_3 and (b) HfO_2 with various ~320 nm thick low ΔH_{ox} metal electrodes. As α_{ECC} scales linearly with κ, the ratio of α_{ECC} values between Al_2O_3 and HfO_2 is approximately equal to the ratio of their dielectric constants, ~8 and ~14, respectively.[3] As discussed above, if the interfaces do not play a role in determining nonlinearity, then α_{ECC} should be independent of d_{ox}. However, the influence of the metal-dielectric interface is clearly seen with α_{ECC} decreasing as d_{ox} decreases. Additionally, different metals show different α_{ECC} values for the same d_{ox}. The influence of the metal-dielectric interface, indicated by the spread in α_{ECC} values between the various metals, is largest for the thinnest dielectrics and decreases with increasing d_{ox}. For the thickest dielectrics, the dependence of α_{ECC} on d_{ox} saturates, and the measured α_{ECC} values of the various metals are closely grouped, indicating reduced influence of the interfaces. As α_{ECC} decreases with decreasing dielectric thickness of both types, the interfaces must be acting to oppose or mitigate α_{ECC} due to the dielectric bulk.

To further investigate the influence of the metal-dielectric interface and the spread on α_{ECC} values between the various metals, plots of C/C_0 versus E are shown in Fig. 2 for the devices with the thinnest dielectrics: (c) 10 nm Al_2O_3 and (d) 11 nm HfO_2. The α_{ECC} values for each metal are tabulated in the insets. The general trend observed for both Al_2O_3 and HfO_2 is the same, with Ag exhibiting the lowest α_{ECC}, followed by the increasing order of Au, Pd, and Ni. Although there is no clear agreement in the literature as to the detailed physical mechanisms responsible for α_{ECC}, a general feature of most models is that the nonlinear changes in capacitance are due to corresponding field induced elastic changes in dielectric thickness, Δd_{ox}. The Δd_{ox} as a function of the electric field may be calculated by modifying the parallel plate capacitor equation

$$\Delta d_{ox}(E) = \frac{\varepsilon_0 \kappa_0 A}{C(E)} - d_{ox}(0\,V) \tag{3}$$

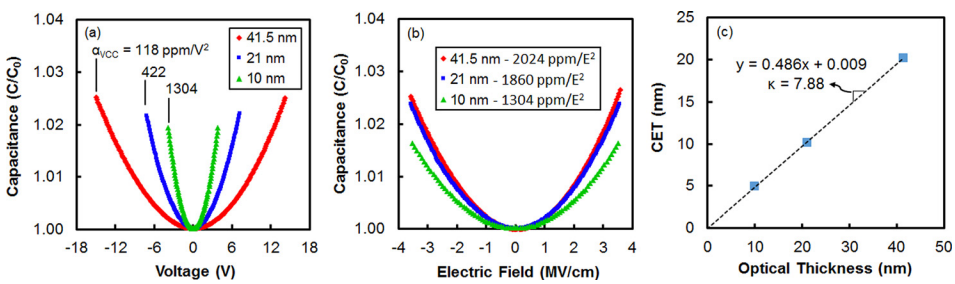

FIG. 1. Normalized baseline adjusted (β term removed) capacitance density vs. (a) voltage and (b) electric field for various thickness Al_2O_3 devices with ~320 nm Ag top contacts. (c) CET (zero-bias) versus measured optical thickness for TaN/Al_2O_3/Ag devices.

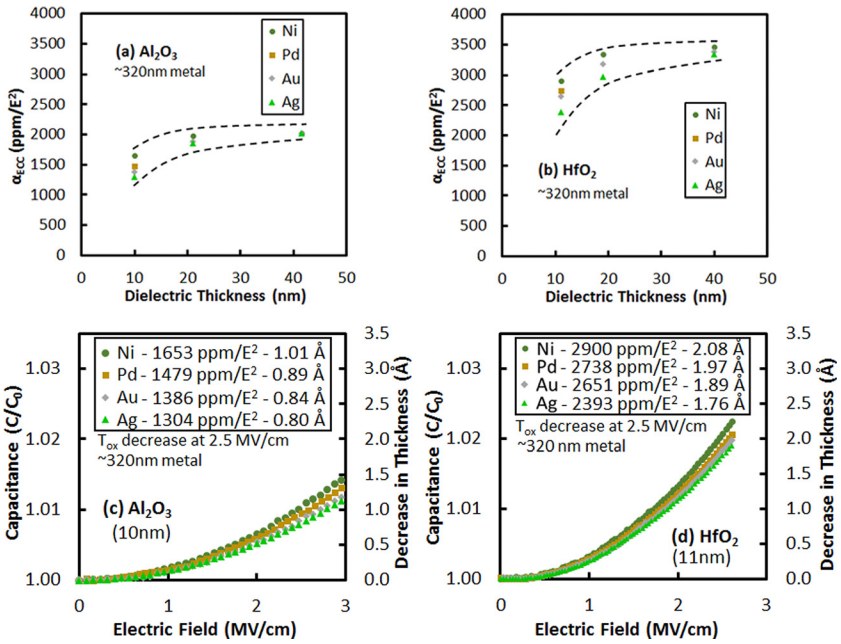

FIG. 2. Plots of α_{ECC} versus dielectric film thickness for ALD (a) Al_2O_3 and (b) HfO_2 with various ~320 nm thick low ΔH_{ox} metal electrodes. Capacitance and calculated decrease in dielectric film thickness vs. electric field for (c) 10 nm Al_2O_3 and (d) 11 nm HfO_2 with various ~320 nm thick low ΔH_{ox} top metal electrodes.

and is shown on the right axis of the plots in Fig. 2. Δd_{ox} values at 2.5 MV/cm are also tabulated in the insets. The ΔC observed for Ni at $E = 2.5$ MV/cm equates to an effective Δd_{ox} of ~1 Å for Al_2O_3 and ~2 Å for HfO_2, which again is roughly proportional to the ratio between their relative κ. The calculated Δd_{ox} range for the various metals is only ~0.2 Å for Al_2O_3 and ~0.3 Å for HfO_2 at 2.5 MV/cm. Although small, this Δd_{ox} variation corresponds to an α_{ECC} range of ~350 ppm/E^2 and ~500 ppm/E^2. We propose that the variation in α_{ECC} observed between the various low ΔH_{ox} metal electrodes in this study is due to an interaction between stress at the metal-oxide interface, caused by the decrease in bulk dielectric thickness, and physical differences between the metal electrodes.

One promising model for positive α_{ECC} materials that predicts an elastic decrease in d_{ox} with applied field was proposed by Wenger *et al.* and employs electrostriction (displacement of ions in the lattice) and Maxwell stress (coulombic interaction of charge between electrodes).[3,23] Under an applied electric field, these mechanisms combine to create a vertical (out of plane) compressive stress which results in a decrease in d_{ox}. The Wenger/compression model is qualitatively consistent with the observation that α_{ECC} scales with κ (see Fig. 2). The ionic bond strength is related to the κ through Coulomb's law. For a given electric field, ionic bonds in high-κ materials are more pliable and thus, experience a greater change than bonds in lower κ materials, resulting in a greater Δd_{ox} and thus greater α_{ECC}.

The compressive deformation within a MIM capacitor for positive α_{VCC} dielectrics is illustrated in Fig. 3 under (a) zero-bias and (b) applied bias. We propose that in addition to vertical compression, the dielectric will attempt to expand horizontally in the x-y plane in order to maintain overall volume.[24,25] This horizontal expansion was not considered by Wenger *et al*. Deformation in non-crystalline solids is by viscous flow,[25] and the horizontal (in-plane) expansion will be inhibited or opposed by the metal-oxide (or even oxide-oxide) interfaces.[22] This results in a horizontal in-plane compressive stress in the dielectric [illustrated by the dashed blue lines in Fig. 3(b)] and a tensile stress in the metal, both concentrated near the interface.

We further propose that restriction of the in-plane expansion in turn restricts the thickness reduction of the dielectric due to applied bias, effectively reducing α_{ECC}. Due to the dielectric stress being concentrated close to the interface, thinner films will exhibit a greater percentage of the dielectric being restricted to in-plane expansion than that of thicker films and thus show even less thickness reduction and further reduced α_{ECC}.[26] The α_{ECC} thickness dependence in Figs. 1(b) and 2, where thinner dielectrics show lower α_{ECC}, is consistent with this interpretation. Because the Wenger *et al.* model considers only the influence of ILOs, rather than the direct impact of the metal/oxide interfaces, it does not predict the thickness dependence of α_{ECC} we observe and cannot account for the differences observed between the various low ΔH_{ox} metals in this study.

Based on this interfacial expansion restriction model, we suggest that the variation in α_{ECC} among the low ΔH_{ox} metal electrodes is the result of differences in the lateral stresses within the dielectric near the electrodes. To explain the small α_{ECC} differences observed between Ag, Au, Pd, and Ni, we must consider the details of the individual metal-dielectric interfaces. The inherent lattice mismatch present at hetero-interfaces may be characterized by a percent lattice mismatch (*f*)

$$f \equiv \frac{a_d - a_m}{a_m}, \tag{4}$$

where a_d and a_m are the dielectric and metal lattice constants, respectively.[27] In layers that exceed the necessary critical thickness to form an extra half plane of atoms, the lattice mismatch typically results in edge dislocations near the interface that relieve strain and reduce surface energy.[26,27] The density of these defects is proportional to the percent lattice mismatch of the interface. Shown in Fig. 3(c) is a simple schematic of an interface between dissimilar materials. Edge dislocations result in localized compression zones (orange)

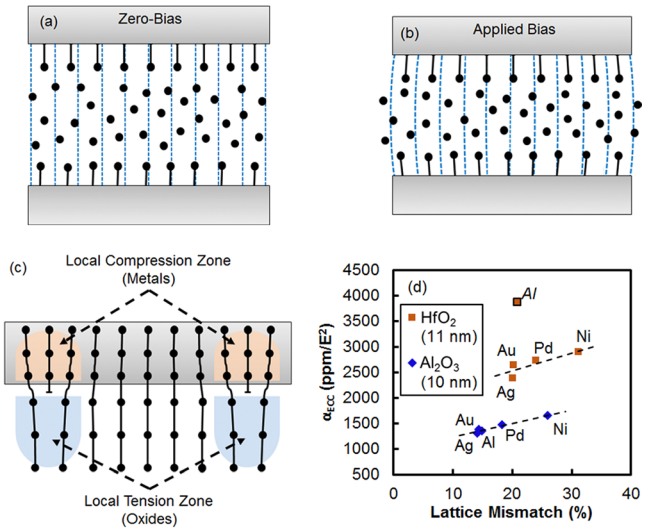

FIG. 3. Cross sectional schematic illustrating (a) before and (b) after elastic deformation (exaggerated) as result of applied bias to a positive α_{VCC} (α_{ECC}) dielectric. Dashed blue lines represent lateral expansion of the dielectric. (c) Schematic of residual stress and edge dislocations at a metal-oxide interface due to lattice mismatch. (d) Plot of α_{ECC} vs. lattice mismatch (f) for Al_2O_3 and HfO_2 with various top metal electrodes.

in the smaller lattice constant material (metal electrode) and localized tension zones (blue) in the larger lattice constant material (dielectric). The stress in these localized zones is opposite to the global in-plane stresses induced by the out-of-plane compression of the dielectric and thus relieves or reduces some of the in-plane stress. Consequently, the differences in α_{ECC} among the low ΔH_{ox} metal electrodes in this study are likely the result of differences in cumulative stress relief due to differing densities of edge dislocations. It is expected that interfaces with increased defect density will experience increased stress relief, allowing more lateral expansion and thus more vertical compression of the dielectric which results in increased α_{ECC}. At the limit, this would mean that a dielectric with no restriction by the electrodes would exhibit the largest α_{ECC}, as there is no restriction to the in-plane expansion of the dielectric as it attempts to maintain volume under applied bias.

Shown in Fig. 3(d) is a plot of α_{ECC} vs. f for Al_2O_3 and HfO_2 with Ag, Au, Pd, and Ni top metal electrodes. f and measured α_{ECC} values are tabulated in Table I for both Al_2O_3 and HfO_2 along with ΔH_{ox} for the metals used in this study.[9,28,29] For both Al_2O_3 and HfO_2, Ag exhibits the least f and smallest α_{ECC} value, followed by Au, Pd, and Ni in increasing order, revealing a direct correlation between f and α_{ECC} for low ΔH_{ox} metals.

For comparison, Al is also included in Fig. 3(d). Al fits the trend for Al_2O_3 but not for HfO_2. This is likely due to the relatively high ΔH_{ox} of Al, which in part drives the formation of an ILO. As discussed earlier, ILO layers can dominate overall α_{ECC}. Due to the high field dropped across a very thin ILO, the α_{VCC} contribution can be very large and lead to a very large overall device α_{ECC} [Eq. (2)]. Indeed, Vallée *et al.* reported that the α_{VCC} of HfO_2 and $BaTiO_3$ devices had roughly a direct relationship with the ΔH_{ox} of the metal electrodes, which is likely the result of ILO formation.[9]

In the case of HfO_2 in this work, α_{ECC} for the Al electrode devices is quite large due to the larger percentage of the electric field dropped across the thin reduced-k ILO formed at the Al/HfO_2 interface. For the Al_2O_3 devices, the formation of an Al_2O_3 ILO at the Al interface is limited[30] and any additional Al_2O_3 that does form will act as single dielectric with slightly increased dielectric thickness. Our results demonstrate that in the absence of ILOs, the f can play a critical role in determining α_{ECC}, especially for the ultrathin dielectrics used for scaling in MIM capacitors for future ITRS nodes.

It is well established that α_{VCC}, the voltage coefficient of capacitance, increases with κ and with decreasing d_{ox}. Most current models of nonlinearity consider only the influence of the "bulk" dielectric, and any ILOs that may be present and typically do not focus on the direct influence of the electrodes. These models predict that in the absence of an ILO, α_{ECC}, the electric field coefficient of capacitance, ought to be independent of d_{ox}. For all of the low ΔH_{ox} metals investigated in this study, we find that α_{ECC} actually *decreases* with decreasing d_{ox}. In addition, different α_{ECC} values are observed for each metal for otherwise identical device structures. Ag exhibits the lowest α_{ECC}, followed in increasing order by Au, Pd, and Ni. Differences between the metals become more pronounced as the dielectric thickness decreases. In order to explain these differences, one must consider the details of the metal/dielectric interfaces. For positive α_{VCC} materials, recent models predict that vertical compression of the dielectric under applied field is responsible for the increased capacitance. We propose that as the dielectric must also expand horizontally to maintain volume, this induces compressive stress in the dielectric and tensile stress in the metal, concentrated near the interface. We further propose that one of the roles of the electrode then is effectively to inhibit the lateral expansion of the dielectric and thus reduce overall α_{ECC}. In confirmation of this model, the α_{ECC} values for both ~10 nm HfO_2 and Al_2O_3 are found to increase roughly linearly with the lattice mismatch of the metal/dielectric interfaces. The interfaces with higher mismatch contain a greater density of edge dislocations that provide increased localized stress relief, which results in a greater cumulative reduction in global interfacial stress and thus allows for increased lateral expansion of the dielectric under applied bias. Finally, a comparison was made with high ΔH_{ox} Al electrodes. While Al fits the trend for Al_2O_3, the Al α_{ECC} is much higher than for the rest of the HfO_2 devices due to the formation of a thin lower-k ILO at the HfO_2/Al interface.

TABLE I. Lattice mismatch (f) and α_{ECC} for Al_2O_3 and HfO_2 with various metals electrodes as well as ΔH_{ox}.

	f-Al_2O_3 (%)	α_{ECC}-Al_2O_3 (ppm/E^2)	f-HfO_2 (%)	α_{ECC}-HfO_2 (ppm/E^2)	Metal ΔH_{OX} (eV/Oxygen)
Ni	25.95	1653	31.11	2900	−2.53
Pd	18.25	1479	23.94	2738	−0.886
Al	*14.91*	*1357*	*20.84*	*3874*	*−5.8*
Au	14.31	1386	20.28	2651	−0.007
Ag	14.16	1304	20.14	2393	−0.311

The ITRS roadmap requires α_{VCC} below 100 ppm/V^2. One way to achieve this is to use multiple dielectrics with complementary material properties, each targeting one or more device attributes.[2,4,31–35] Using this approach, increased C with low leakage J can be obtained while simultaneously minimizing α_{VCC} through the "cancelling effect".[2] The cancelling technique uses two or more dielectrics in a stack with at least one dielectric exhibiting a positive sign α_{VCC} and another exhibiting a negative sign α_{VCC}. By carefully controlling the thickness of each dielectric layer, their individual contributions to α_{VCC} cancel one another; the overall device nonlinearity may be minimized. For the low ΔH_{ox} metals in this study, α_{ECC} increases with increasing d_{ox}, saturating for thick oxides. As thinner dielectrics are used to achieve higher C, the metal electrodes exert influence over a greater percentage of d_{ox}. We have shown that even for 10 nm dielectrics, the electrode can already influence α_{VCC} by more than 500 ppm/V^2, and therefore must be considered. Thus, although secondary to the dielectric properties and thickness, the electrodes will become more critical and strategies such as the canceling approach will become more difficult to implement.

This understanding of the impact of the metal electrodes on nonlinearity should aid in rapid scaling and optimization of low α_{VCC} MIMCAPs. The lattice mismatch and mechanical influence of the electrodes have not been considered previously and may light a path to future improvements in nonlinearity. For example, our results suggest that minimizing the lattice mismatch between the dielectric and metal electrodes or mechanically pinning the interface may be strategies worth investigating to produce highly scaled devices with ultra-low α_{VCC}.

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